Digital Multimeter IC “HAZ01”

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***Abstract*—Hioki developed the HAZ01, a CMOS mixed-signal IC, for use in the Digital Multimeter DT4220 and DT4250 series, which are based on the concept doing a professional job quickly. This paper discusses the HAZ01's features, functionality, architecture, and characteristics.**

I. Introduction

Digital multimeters are basic tools that provide a range of functionality in a single instrument, including voltage, current, and resistance measurement capability. Internally, they consist of a dedicated IC that is responsible for measurement along with a microprocessor that is responsible for the display of measured values and user interface functionality. Improving the performance of the dedicated IC is an essential task in the effort to meet the full range of user requirements, where priorities include compact size and low cost in addition to high stability and fast response.

II. Overview

TABLE I provides an overview of the HAZ01. Hioki chose a 0.25 μm CMOS process from the standpoint of balancing performance and cost. With the exception of the pre-process, production and testing are all carried out in Japan in order to maintain the highest possible level of quality.

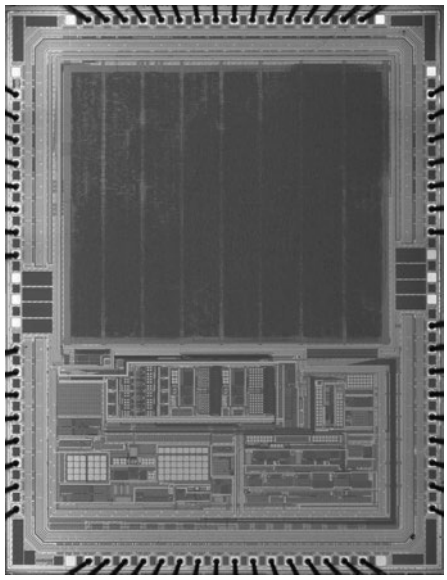
III. Functions and Features

1) High stability

To improve system performance, a high-precision, low-noise A/D converter is essential. Hioki chose a ΔΣ type that yields high resolution since it is a natural fit with the CMOS process and developed an A/D converter with a resolution of 16 bits and a sampling rate of 10 kS/sec. A digital calibration function eliminates offset and gain drift, delivering a high level of stability.

2) Fast response

The RMS value calculation unit consists of a digital computing subunit and a digital filter, rather than an analog RMS-DC converter and analog filter. This design increases the degree of freedom characterizing calculations and filtering, enabling fine-grained calculation control. The resulting ability to optimize characteristics in response to measurement conditions, for example by switching to the fast-response filter during auto-range operation and then switching to the high-stability filter once the range has been determined, allows the IC to deliver both fast response and high stability.



Appearance of the HAZ01 Chip

TABLE I. HAZ01 Overview

Characteristic	Specifications	
Process	CMOS	
Minimum gate length	0.25 μm	
Circuitry	Mixed analog/digital	
Supply voltage	Analog I/O	3.3 V
	Digital	2.5 V
Clock frequency	2.56 MHz	
Package	LQFP64-10X10-0.5 (RoHS compliant)	
Current consumption	Approx. 4 mA	
Analog input	±1.5 V	
A/D converter	ΔΣ type, 16-bit, 10 kS/sec.	
Calculations (number of bits, refresh speed)	RMS/mean (24 bits, 10 times/sec.) BAR (11 bits, 80 times/sec.)	
Dynamic range	6,000 counts Crest factor: 2.5	
Functionality	ACV, DCV, ohm, continuity, capacitance, peak, etc.	

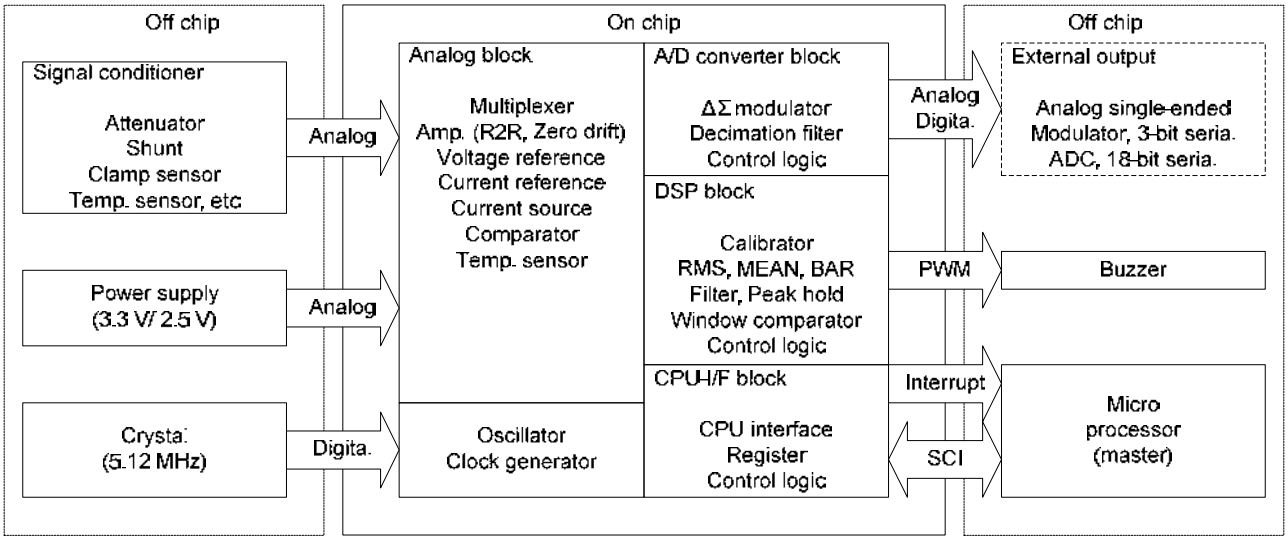


Fig. 1. Overall Block Diagram

3) Multifunctional analog circuit

All circuitry needed for a digital multimeter has been implemented on the chip, including basic circuitry, a multiplexer, a reference voltage source, a current source, a temperature sensor, multiple amps, a comparator, and an A/D converter. This approach simplifies the design of the digital multimeter’s peripheral circuitry and reduces the number of parts in the instrument.

4) Simultaneous RMS/mean measurement

The chip simultaneously calculates RMS and mean values. This approach not only allows the dual display of RMS and mean values, but also makes it possible to automatically detect whether a given current is AC or DC by measuring the three parameters of AC + DC (RMS), DC, and AC and carrying out calculation (1) externally.

$$AC = \sqrt{RMS^2 - DC^2} \tag{1}$$

5) Digital peak hold function

By using the digital peak hold function, it is possible to measure rush voltage/current and ripple voltage/current superposed on DC.

6) Filter function

The chip incorporates a variable-passband 100 Hz/500 Hz digital filter, which makes it possible to reduce carrier effects in inverter fundamental wave measurement.

7) Power-down function

The ability to power down unused circuits or the entire chip helps limit power consumption.

8) Capacitance measurement function

The chip incorporates functionality for performing DC charge/discharge capacitance measurement and provides a discharge detection circuit using an integrated analog comparator. By detecting when the capacitor being measured is discharged completely and automatically controlling the discharge circuit, over-discharge—in other words, reverse bias to the capacitor—can be prevented. In addition, this approach means the off-chip CPU need only control the start of charging and discharging. Furthermore, with a digital comparator, the charge/discharge voltage can be set freely. The ability to optimize the charge/discharge voltage based on the capacitance of the capacitor being measured can be expected to reduce measurement times and improve measurement precision.

IV. Architecture

A. Hardware Architecture

Fig. 1 provides an overall block diagram. The chip consists of an analog block, A/D converter block, digital signal processing (DSP) block, and CPU-IF block, which is responsible for the interface with the off-chip CPU.

B. Analog Block

1) Multiplexer

Hioki has enabled a four-terminal connection for the switch for the external resistance attenuator architecture (1/10000, 1/1000, 1/100, 1/10) to reduce the effects of on-resistance and wiring resistance. In addition, the chip provides eight switching channels for low-voltage direct input.

2) Reference voltage source

The chip provides a band gap reference (BGR) type constant-voltage generation circuit that serves as the IC’s internal reference voltage source and as the reference voltage source for the A/D converter. Key design considerations included the balance of temperature characteristics, flicker noise, mounting area, and current consumption. Furthermore, Hioki made it possible to supply the reference voltage from an external source in order to obtain stable characteristics.

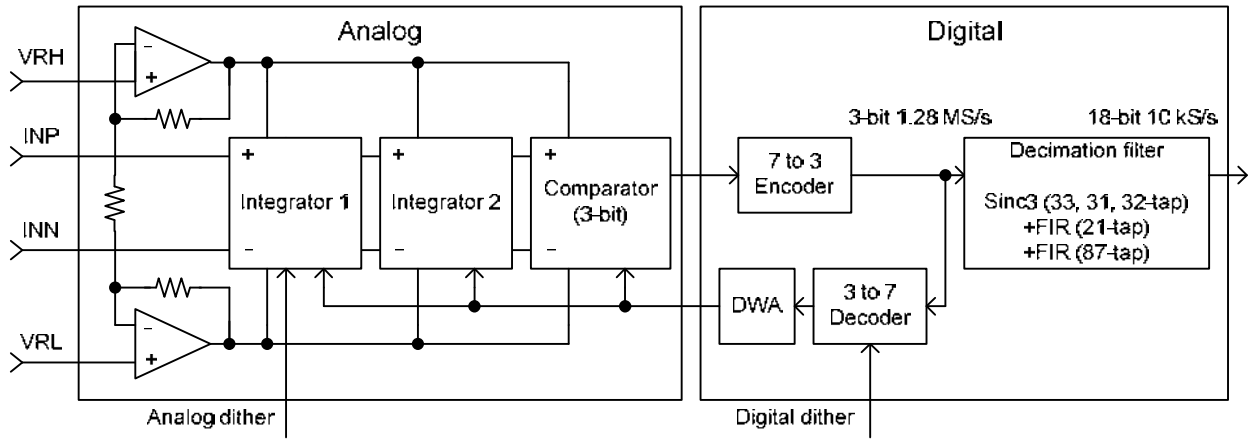


Fig. 2. A/D Converter Block Diagram

3) Constant-current source

The chip provides a constant-current generation circuit for resistance measurement, capacitance measurement, and continuity check use. The chip is able to regulate current values (10 nA, 100 nA, 1 μA, 10 μA, 100 μA, and 200 μA) and uses pulse width modulation (PWM) to achieve currents of less than 1 μA.

4) Amps

Amp use is determined based on the location of use. A rail-to-rail amp is used for the initial stage in order to secure adequate dynamic range, even for a supply voltage of 3.3 V. A switching zero-drift amp is used in locations where input impedance and input leak current will not have any effect, for example for internal reference. Finally, a full differential amp is used to drive the A/D converter in order to improve the dynamic range and common-mode rejection ratio (CMRR).

5) Comparator

The chip provides a comparator for waveform shaping during frequency measurement. By giving the comparator hysteresis characteristics to enable reliable shaping even in the presence of superposed noise and using an internal attenuator (1/2), the hysteresis width can be doubled. This design can accommodate frequency measurement of up to about 200 kHz.

C. A/D Converter Block

1) ΔΣ modulator

Fig. 2 provides a block diagram for the A/D converter. To ensure adequate S/N characteristics with low power consumption, Hioki chose a 3-bit, second-order ΔΣ modulator. The theoretical S/N ratio is 144 dB with 128× oversampling. The ΔΣ modulator also provides a data weighted averaging (DWA) function to reduce characteristic degradation due to the 3-bit comparator's non-linearity and a dithering function to prevent limit-cycle oscillation.

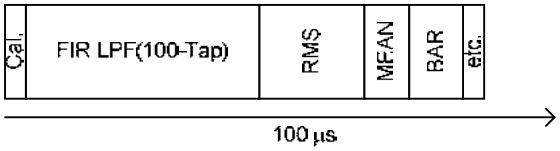


Fig. 3. FPU Time-sharing Control in the DSP Block

2) Decimation filter

It is necessary to lower the data rate from 3-bit 1.28 MS/sec. data to 18-bit 10 kS/sec. data by means of a process known as decimation. Hioki designed a three-stage process to increase the circuit's efficiency. The first stage comprises sinc3 filters of 33, 31, and 32 taps to obtain band stop characteristics using the SINC filter's notch. The second and third stages comprise finite impulse response (FIR) filters, with the third-stage FIR filter compensating for the sinc3 filters' attenuation to ensure a flat pass band.

3) External output

The 3-bit and 18-bit data from the ΔΣ modulator and A/D converter, respectively, can be output from the chip. This data can be used to record and display waveforms.

D. DSP Block

1) Calibration unit

The calibration unit provides a calibration function designed to eliminate offset errors and gain errors from its circuitry, including the A/D converter. The calibration unit supports command control from the off-chip CPU. It performs calibration in as little as 12.5 ms and is designed to minimize loss time relative to the display refresh rate of 100 ms.

2) RMS calculation unit

The RMS calculation unit is responsible for all root mean square (RMS) calculations. A single floating-point unit (FPU) is shared by means of time-sharing control, allowing the size of the circuit as well as its current consumption to be reduced. The design provides a low-pass filter to reduce ripple after square calculation as well as a window function multiplier to reduce clipping error. Fig. 3 illustrates how time-sharing control of the FPU operates. All

required calculations are performed in real time after each A/D converter sampling cycle. The architecture is capable of completing all calculations within the sampling period of 100 μs, even under the maximum calculation load when using a 100-tap (bandwidth of 100 Hz) FIR filter (explained below).

3) Mean value calculation unit

The mean value calculation unit allows selection of the simple mean (DC mean value) or the absolute mean (AC mean value). The design includes a filter and window function multiplier.

4) Bar graph calculation unit

The calculation unit responsible for preparing data for bar graphs allows data to be refreshed as quickly as 12.5 ms. Either RMS values or mean values can be selected.

5) Filter unit

Broadly speaking, the DSP block has two types of digital filter. The first, known as the pre-filter, has been inserted before the square circuit to limit the measurement signal band. The second, known as the post-filter, has been inserted after the square circuit to reject ripple occurring after square calculation. Since the design is required to exhibit stability in response to all possible signal input, including, for example, transient response to noise and during range switching, Hioki chose an FIR filter as the pre-filter and a first-order infinite impulse response (IIR) filter as the post-filter and connected them in a cascading arrangement. The pre-filter’s pass band can be set to either 100 Hz or 500 Hz, and the post-filter’s cutoff frequency and number of orders can be changed.

6) Peak hold unit

The chip provides a peak hold circuit using data that is output every 100 μs by the A/D converter, just as with measured value calculation. The circuit can hold rush waveforms and ripple peak values with a refresh rate of 100 ms. Since it consists of digital circuitry, the unit operates in a stable manner that is free from the effects of temperature drift and leak current.

7) Window comparator

The chip provides a window comparator and associated interrupt output. Use of digital control enables the window width to be changed freely as desired. This circuit also implements the continuity check function. In addition, it can be used to perform frequency measurement of low frequencies that can be measured using 10 kS/sec. data and duty ratio measurement, and it is used in capacitance measurement.

E. CPU-IF Block

1) Interface

The chip provides a three-wire serial interface and various interrupts for use in communicating with the CPU. Communication clock speeds of up to 320 kHz are supported.

2) Command control

To simplify control from the CPU, function and range settings can be manipulated by means of both command control and bit control.

V. CHARACTERISTICS

A. Voltage Dependence of Analog Switching Characteristics

Fig. 4 illustrates the voltage dependence of the on-resistance and leak current of the analog switches that make up the multiplexer. The multiplexer utilizes two types of switches: a ΔΩ design with reduced on-resistance voltage dependence and a low-leak design with reduced leak current. Although the leak current values shown in the figure include the leak current for the input protective diode and two types of analog switches, they are nonetheless limited to ±10 pA or less in the operating voltage range.

B. Linearity of the Rail-to-rail Amp

Fig. 5 illustrates the linearity of the rail-to-rail amp, which provides precision of ±0.1%. Errors equal to or exceeding ±1.2 V are caused by the design of the rail-to-rail amp’s input block, which consists of two P-type and N-type differential pairs. The amp switches between the P-type differential pair and the N-type differential pair depending on the input voltage, allowing it to operate up to the supply voltage. Crossover distortion and offset voltage fluctuations occur at the point at which the amp switches between the two differential pairs. Commercially available rail-to-rail amps (values for which are indicated by Samples 1 and 2 in Fig. 6) exhibit similar characteristics, which are unavoidable due to the amp’s design.

C. Decimation Filter Frequency Characteristics

Fig. 7 illustrates the overall frequency characteristics for the decimation filter, while Fig. 8 provides an expanded view of the shoulder-shaped portion of the frequency characteristics. Hioki chose approximately 3 kHz as the pass band where stability is emphasized. By compensating for the sinc3 filters’ attenuation with the FIR filter, pass band ripple has been limited to ±0.05% (±0.00434 dB).

D. Pre-filter Frequency Characteristics

Fig. 9 illustrates the characteristics of the pre-filter that is used to limit the measurement signal band. Pass bands are 100 Hz, 500 Hz, and 3 kHz (the A/D converter’s decimation filter band).

E. Post-filter Frequency Characteristics

Fig. 10 illustrates the characteristics of the ripple rejection post-filter after square calculation. While LPF characteristics are obtained during 100 ms averaging processing (labeled “Default” in the figure), greater attenuation can be obtained by adding an LPF. The graph makes it clear how attenuation characteristics of second and

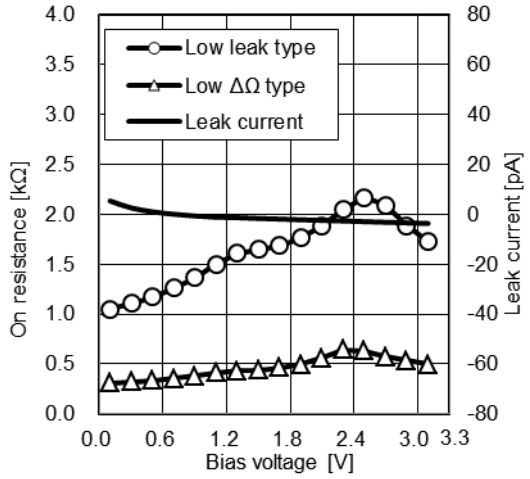


Fig. 4. Voltage Dependence of Analog Switch On-resistance and Leak Current

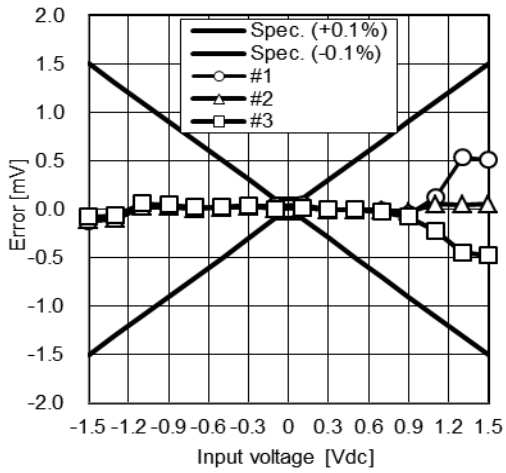


Fig. 5. Rail-to-rail Amp Linearity

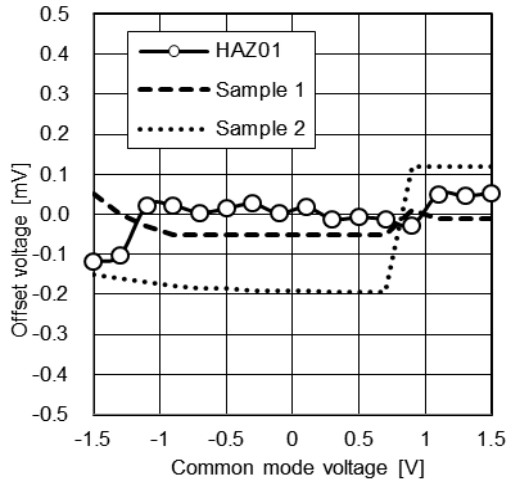


Fig. 6. Rail-to-rail Amp Offset Voltage/Common Mode Voltage Characteristics

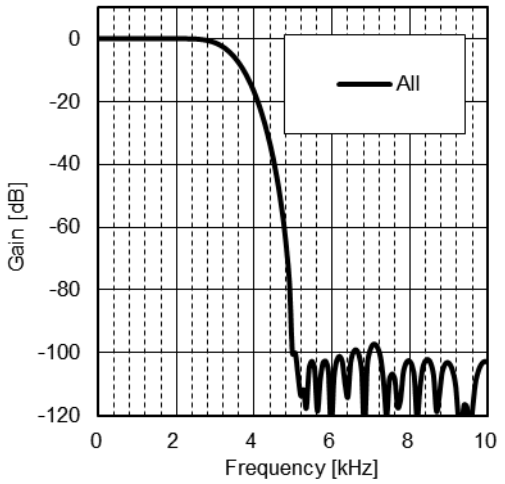


Fig. 7. Decimation Filter Overall Frequency Characteristics

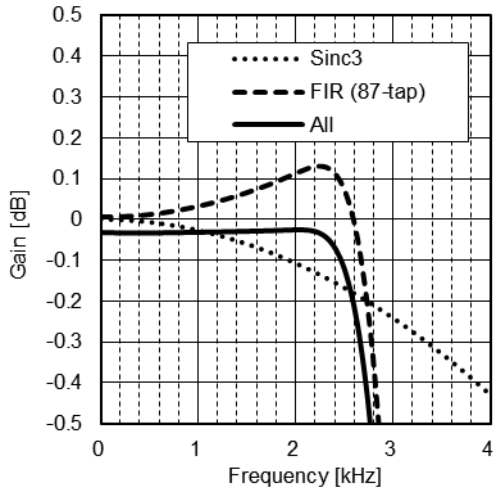


Fig. 8. Decimation Filter Frequency Shoulder Characteristics

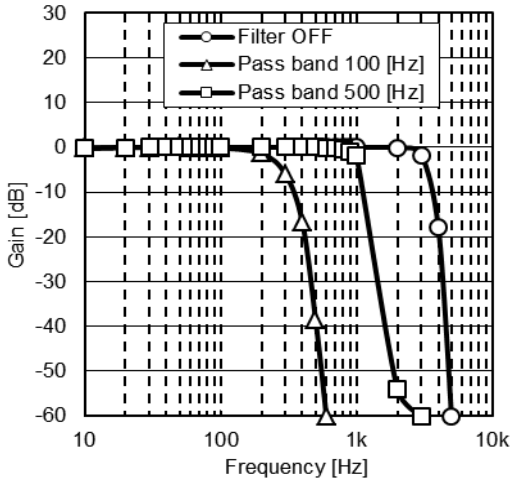


Fig. 9. Pre-filter Frequency Characteristics

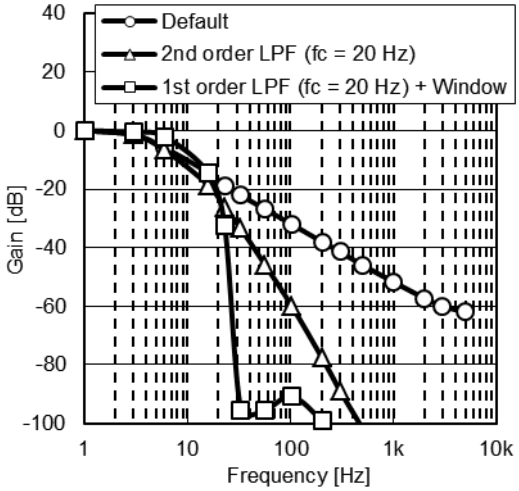


Fig. 10. Post-filter Frequency Characteristics

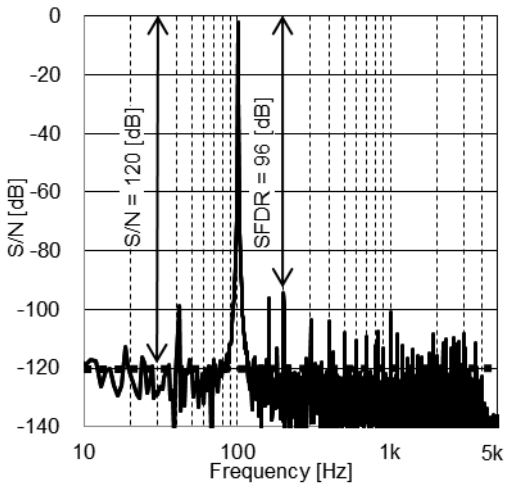


Fig. 11. FFT Analysis of A/D Converter Output

higher orders can be obtained even with a first-order filter by further adding a windowing calculation.

F. A/D Converter S/N Ratio

Fig. 11 illustrates the results of an FFT analysis of the A/D converter’s output when fed sine wave input (600 mV rms, 100 Hz). The S/N ratio (i.e., the ratio of signal to the noise floor) was about 120 dB, and the spurious free dynamic range (SFDR) was about 96 dB.

G. System Linearity

Fig. 12 illustrates the overall system’s linearity, indicating that a precision of ±0.1% is assured for the system overall. The error at ±1.2 V or greater is the previously described rail-to-rail amp’s offset voltage error.

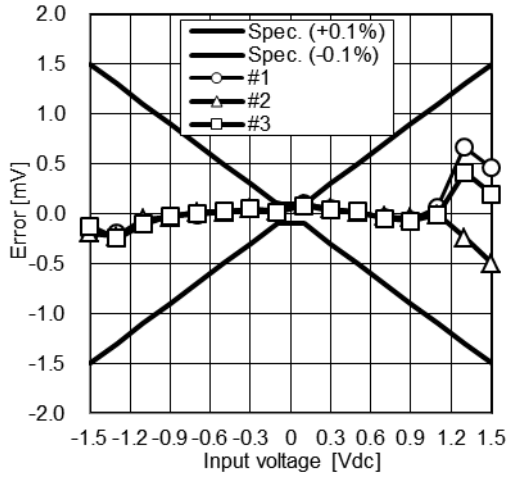


Fig. 12. System Linearity

H. System S/N Ratio

Fig. 13 illustrates the relationships between the overall system’s S/N ratio and the effective number of bits (ENOB). The overall system’s S/N ratio (indicated by circles in the figure) is about 120 dB, which is equivalent to 19 effective bits and which more than achieves Hioki’s target of 16-bit precision. Spurious free dynamic range (SFDR) (indicated by triangles in the figure) exhibits some degradation caused by the linearity of the previously described rail-to-rail amp, but 16-bit precision is still maintained up to the ordinary amplitude range (crest factor: 1.5) of 1.8 Vpp. In addition, a minimum of 60 dB (0.1% or less) is maintained up to the input range upper limit of 3 Vpp, along with adequate SFDR performance.

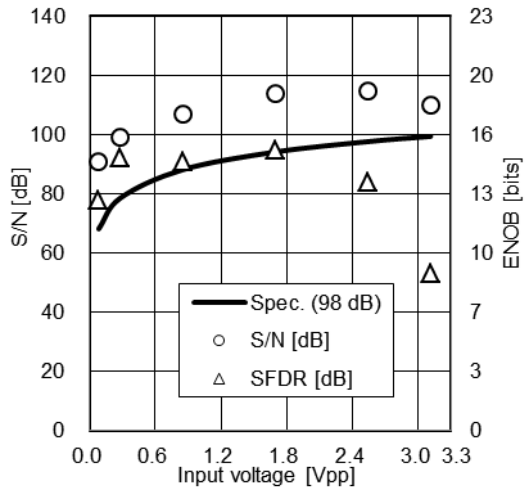


Fig. 13. Input Amplitude and S/N Characteristics

VI. Conclusion

Hioki developed the HAZ01 CMOS mixed-signal IC to balance a wide range of functional and design requirements in a sophisticated manner. Going forward, the company plans to use the design in numerous models.

Hioki would like to express the team’s gratitude to the many people who cooperated with this project by lending the company their insight and guidance, including its development partners; the late Michio Okamura, whose support was invaluable; Associate Professor Yuji Izawa of Shinshu University; Associate Professor Kohji Higuchi of the University of Electro-Communications; Professor Akira Yasuda of Hosei University; and Professor Takanori Komuro of the Kanagawa Institute of Technology.

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